Cloud Testing Service External Power Supply Control

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Outline

- Existing Verification Environment @Xilinx
- Cloud Testing Service Approach
- Power Control Requirements
- Power Supply Control Implementation
- Xilinx-CTS Collaboration
- How "The New Pattern Verification" Environment Works
- Next Steps, Q&A and Wrap-up



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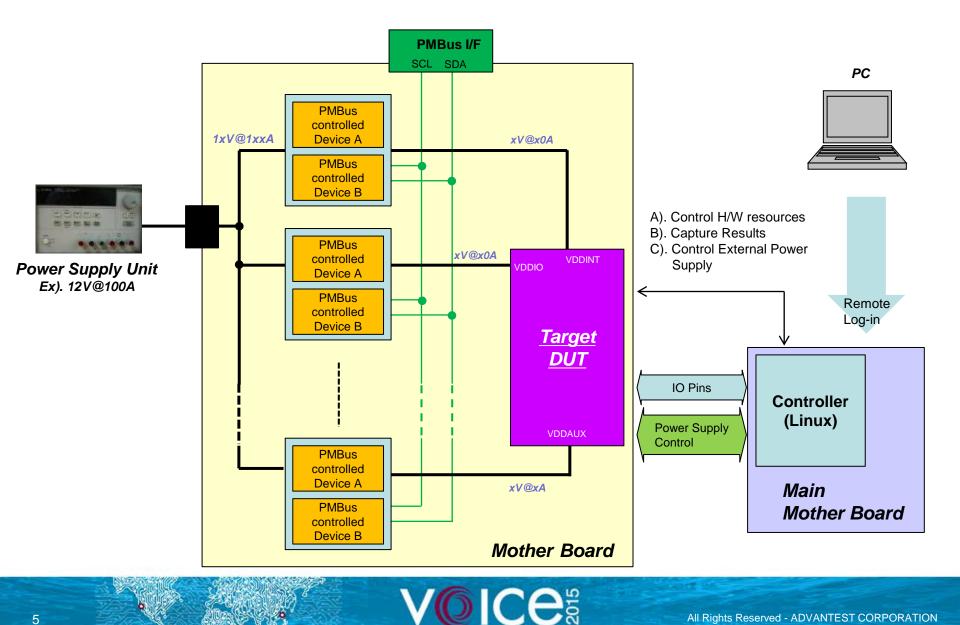


Existing Evaluation Environment @Xilinx

- Remote Log-in to Mother Board Computer from User PC's.
- Operating System on Mother Board is Linux
- Mother Board issues Commands/Script for controlling Mother Board
 - HW Resources (Digital Pins, Pattern Execution)
 - Power Supply Units
 - Capture PASS/FAIL Result, Power Supply Current, etc.
- Does not use PMBus I/F connector on the Mother Board.
- There are two types of Power control device via PMBus on Mother Board
 - Device A \rightarrow Voltage Regulator
 - Device B \rightarrow Current Measurement



Existing Evaluation Environment



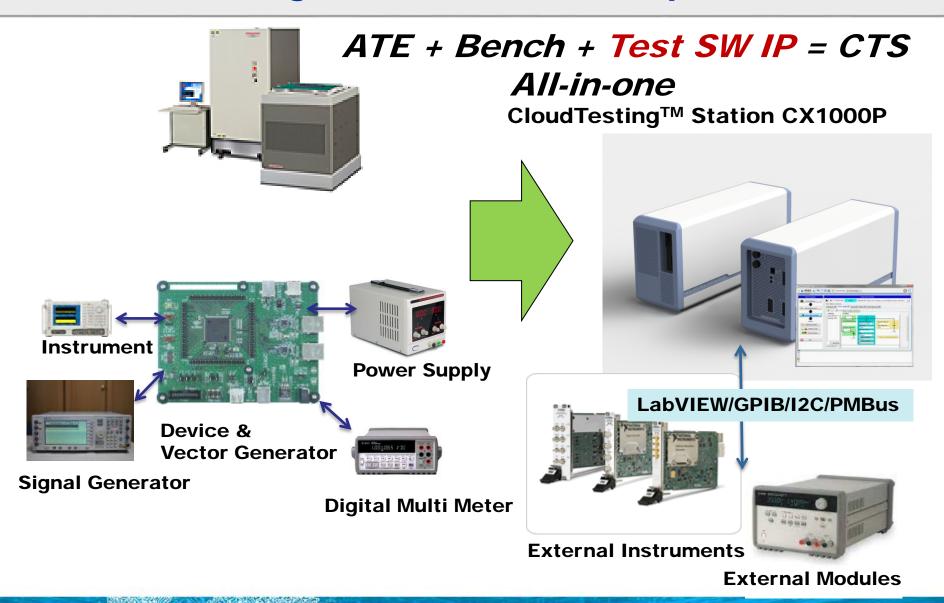
- Faster Pattern Execution
- Capability to Shmoo Power vs Frequency
- Easy Failure Analysis with LVP (Laser Voltage Prober)
- Modify Timing Levels & Pattern to Debug DUT
- Easy Maintenance of Hardware



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Cloud Testing Service - HW Concept

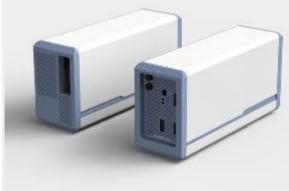


Cloud Testing Service - Usage



CTS - Hardware Models To Choose From





I/O: 32ch DPS: 2ch PMU: 1ch AWG: 1ch DGT: 1ch RVS: 2ch

CX1000D

I/O: 128ch DPS: 8ch PMU: 4ch AWG: 4ch DGT: 4ch

RVS: 8ch

- 1. Small Footprint
- 2. Air Cooled
- 3. Office Power Outlet 100V-240V
- 4. Configurable Architecture
 - MCU
 - FLASH

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CX1000D S2-LINK

I/O:	256ch	AWG:	8ch
DPS:	16ch	DGT:	8ch
PMU:	8ch	RVS:	16ch



Flash Memory Test (Firmware Upgrade)

<u>CX1000P</u>

I/O: 32ch DPS: 2ch PMU: 1ch RVS: 2ch ALPG: 200/ 400 Mbps



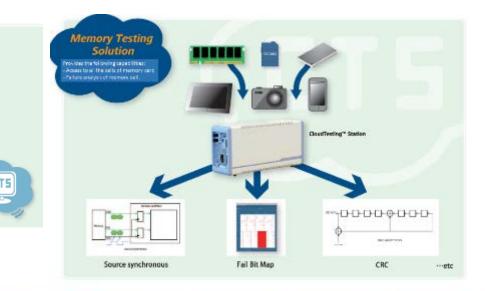
I/O: 128ch DPS: 8ch PMU: 4ch RVS: 8ch ALPG: 200/ 400 Mbps

[To access entire address space of memory card]

- Read/Write the memory at max rate of 400Mbps.
- The ALPG is compatible with Advantest memory tester T5xxx.
- Test any size memory by single data path.
- Built-in Source Synchronous Test capability.

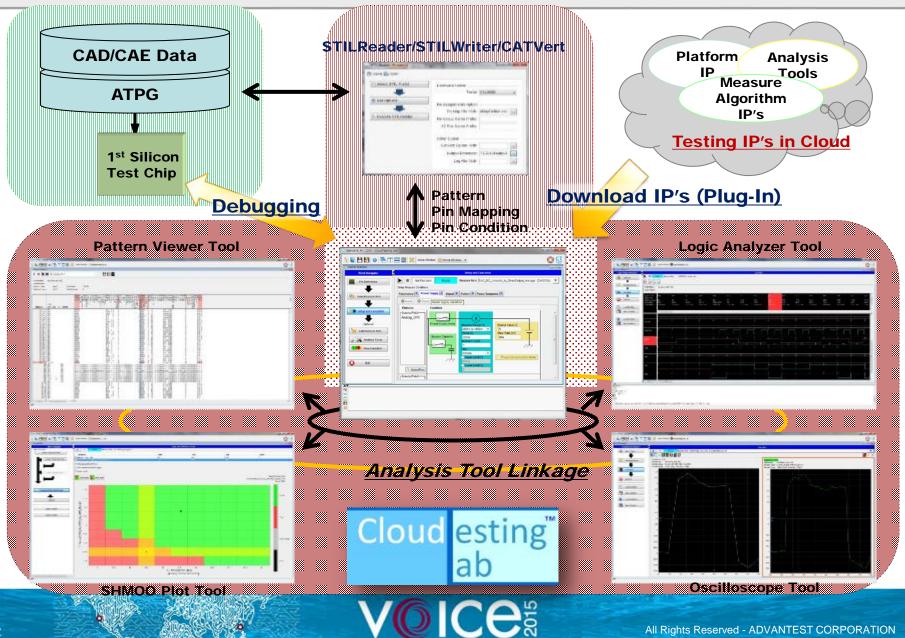
[Failure analysis environment for memory has]

- 32 GB of failure analysis memory.
- Generates CRC for SD card and MMC.
- Drive/compare 1MB of random and deterministic data.
- Test/Skip failing blocks of Flash memory.





Interactive GUIs Connecting Everything



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Power Control Requirements

- Integrate PMBus I/F protocol in CX1000D system
 - Two new custom software for controlling the external power supply via I2C I/F
 - Define Voltage condition parameter via PMBus command
 - Check PMBus status via PMBus Command
- Implement PMBus alert signal to check using LED circuit on I/F Board.
- Implement voltage regulator power on/off via external relay unit.
- Support voltage regulator devices control via PMBus I/F.
- Provide Seamless GUI For Power vs Frequency Shmoo



What's PMBus?

PMBus

Items	Value	Comment
Revision	Rev 1.2	Based on PMBus 2.0
Clock Speed	100KHz	CX1000D has 100KHz I2C I/F
Pin Count	PMBCLK PMBDATA PMBALERT PMBCTRL	I2C SCL I2C SDA Control On/Off via Relay on Mother Board

Command Lists

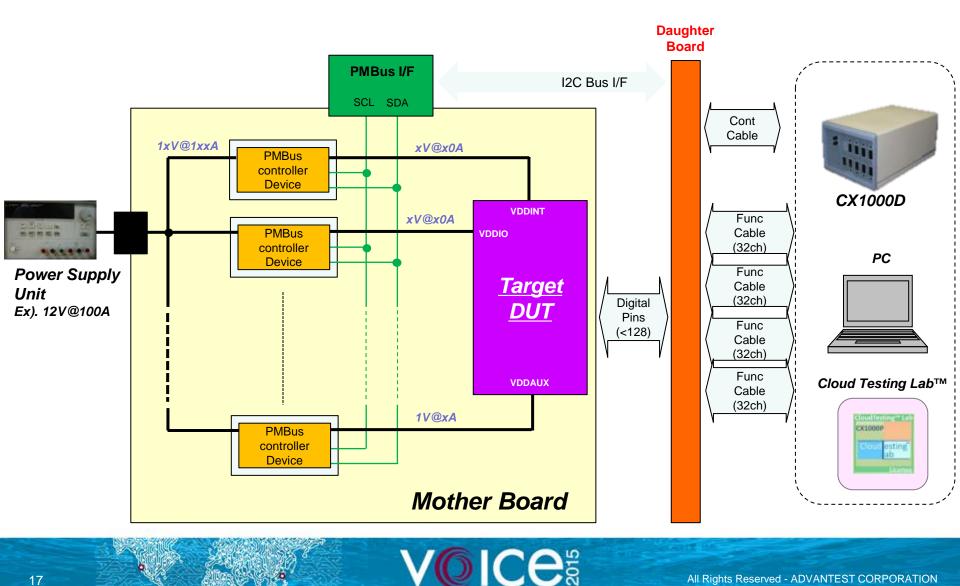
CAL_GAIN	POWER_GOOD_ON	READ_VOUT
OV_FAULT_LIMIT	POWER_GOOD_OFF	READ_IOUT
UV_FAULT_LIMIT	STATUS_WORD	READ_TEMPERATURE_1
DC_FAULT_LIMIT	STATUS_VOUT	READ_TEMPERATURE_2
/_FAULT_LIMIT	STATUS_IOUT	
/_FAULT_LIMIT	STATUS_INPUT	
ELAY	STATUS_TEMPERATURE	
ISE	STATUS_CML	
DELAY	STATUS_OTHER	
FALL	READ_VIN	
	DV_FAULT_LIMIT JV_FAULT_LIMIT C_FAULT_LIMIT _FAULT_LIMIT _FAULT_LIMIT ELAY SE DELAY	DV_FAULT_LIMIT POWER_GOOD_OFF JV_FAULT_LIMIT STATUS_WORD C_FAULT_LIMIT STATUS_VOUT _FAULT_LIMIT STATUS_IOUT _FAULT_LIMIT STATUS_INPUT ELAY STATUS_CML SE STATUS_CML DELAY STATUS_OTHER

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CX1000D: Interface Block Diagram



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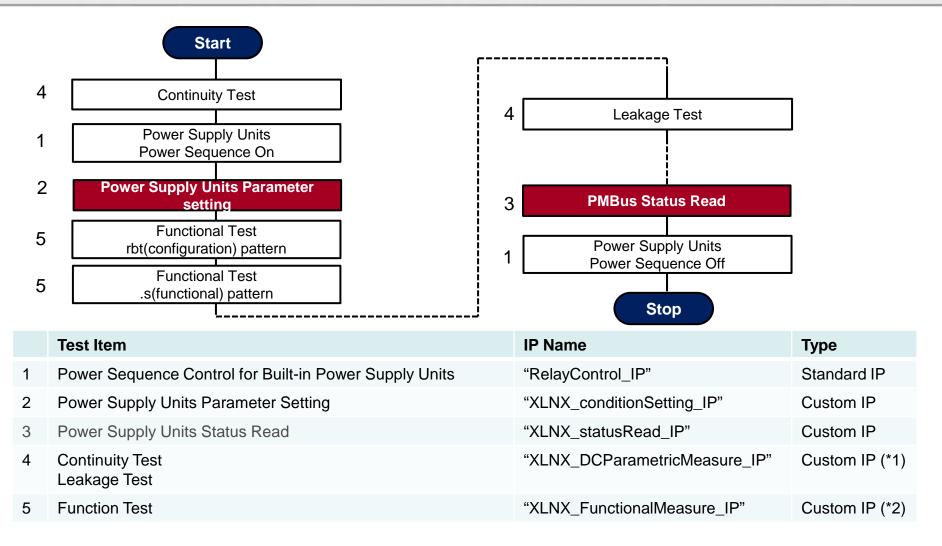


CTS Xilinx Collaboration

- Software High Level Spec Xilinx + CTS
- Interface Board Design & Fab Xilinx.
- PMBus IP Design & Implementation CTS.
- Bring up of Test Flow Xilinx + CTS.



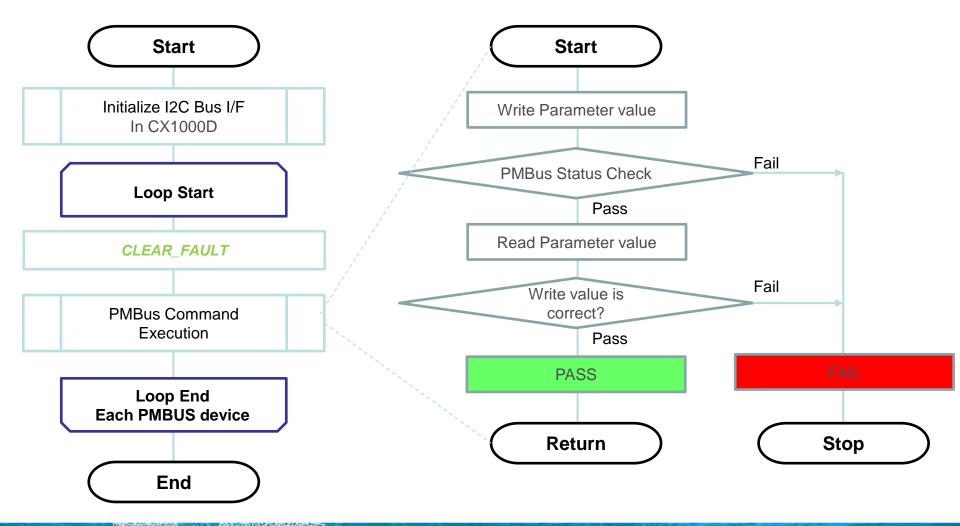
Software Specification



- *1. Required all of Power Supply Unit pins are opened.
- *2. Shmoo execution is available on this IP's

Software Specification

PMBus Command, the execution sequence





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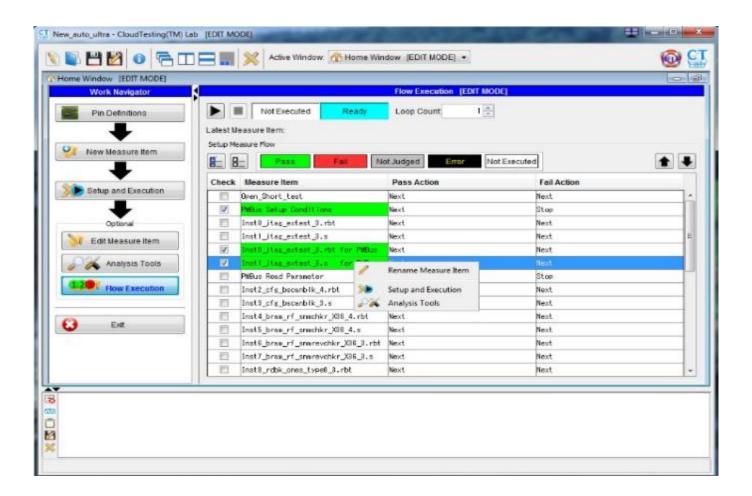


CX1000D Test Condition Image

Setup M	Not Executed	Ready	Measure llem. Pl	NBus Setup Conditions - [XLNX_conditionSettin	0_IP1	•
Insert	Add Delete 🛧 🖡	import 🙀	Export			📰 Fail Stop 📰 Trace Lo
index	Pin Name	Slave Address	Device Type	Condition	Status	Comment
	IVCCENT	0×70	VT7701M	0.95 0 1.52 1.52 0.25 60 0 600 0 4 2	Read/	MCCINT ØYT7701M
	2 VCCAUK	0×08	WAX15361	1.8 8 3 4 8.2 3 8 600 8 12 12 12 12	Ready	MCCAUX @MAX15301
	3 VCCNIK_10	0×0E	WAX15381	1.8 8 3 4 8.2 1 8 600 8 12 12 12 12	Finado	MCCAROLID RMAX15301
	4.VCCBRAN	0×0F	WAX1530.1	0.95 0 2.5 4 0.2 5 0 600 0 12 12 12 12	Ready	VCCBRAN ONAX15301
	5 VCCD_HRA	0x11	WAX15201	1.8 0 3 4 0.2 3 0 600 0 12 12 12 12	Ready	MCCO_HEA @WAX15301
	6 VCCO_HRB	0×12	MAX15301	3.3 0 5 5 0.2 3 0 600 0 12 12 12 12	Resdy	MCCO_HRE @WAX15301
	7 VCCO_HPA	0×13	MAX15301	1.0 0 3 4 0.2 3 0 600 0 12 12 12 12	Ready	VCCO_HPA @WAX15301
	8 VCCO_HP9	6×14	WAX15301	1.5 0 3 4 0.2 3 0 600 0 12 12 12 12	Read/	YCC0_HPB 0WWX16301
	9 MGTANCC 0 MCTANTT	0×15 0×16	MAX15301 MAX15301	1 0 2.5 4 0.2 12 0 600 0 12 12 12 12	Ready	METAVCE ENAX15301 METAVTE ENAX15301
	1 MGTVCCAUX	Ex18	MAX15301 MAX15301	1.2 0 0 4 0.2 12 0 000 0 12 12 12 12 1.8 0 3 4 0.2 1 0 600 0 12 12 12 12	Firsch/ Firsch/	HETVICAUX ONAX15301
	2 UTIL_1V8	6×19	W4X15301	1.8 8 3 4 6.2 1 0 600 0 12 12 12 12	Ready	UTIL 1V8 ONAX15301
	2 UT1L_2Y5	0x14	MAX15281	2,5 0 5 5 0,2 2 0 600 0 12 12 12 12	Feady	UTIL_2V5 @NAX(15301
	4 UT1L 3Y9	0x18	MAX15381	3.3 8 5 5 6.2 5 8 600 0 12 12 12 12	Ready	UTIL 3V3 0NAX15301
	5 UT1L 540	0x1C	WAX15301	5 0 5.5 5.5 0.2 5 0 800 0 12 12 12 12	Ready	UTIL 5V0 0WAX15301
VIN val	ue 12.00 [M] : V	IN Range 11.00	M : VIN damp	(+) 12.50 [M] : VIN clamp(-) 6.50 [N	9	

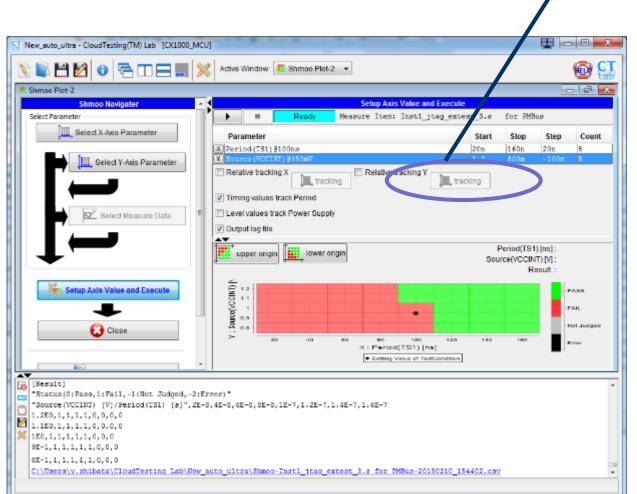


CX1000 Flow Image

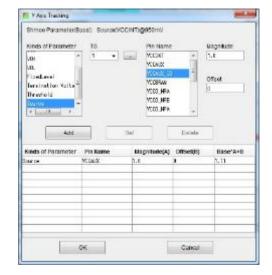




CX1000 Shmoo Image

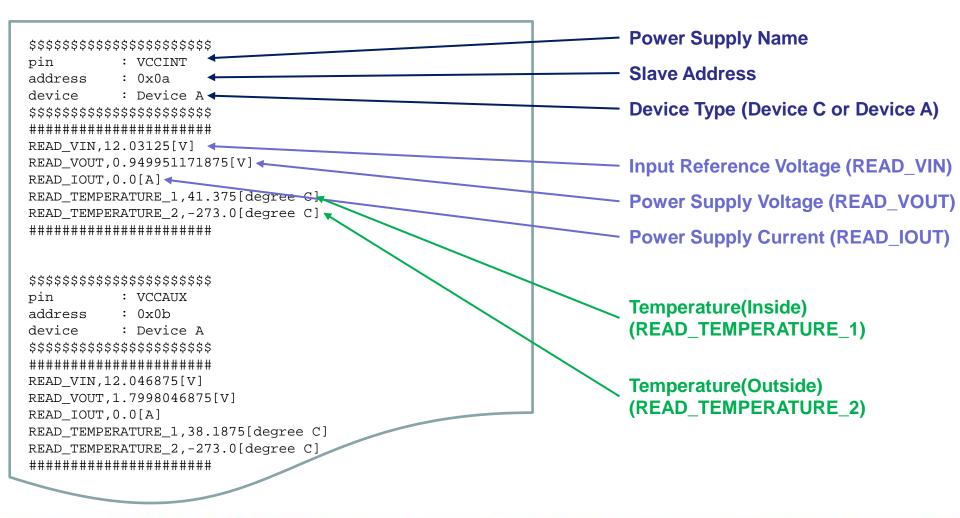


Select another Power Supply Tracking



Check condition from Built-in Power Supply

Log Format





CTS VS Xilinx Board Testing Environment

- Portable Small Foot Print, Powered from wall outlet.
 ✓ Easy Failure Analysis with LVP (Laser Voltage Prober).
- Expandable Easy to add many capabilities.
- No Maintenance Charges Replacement unit shipped free.
 ✓ Easy Maintenance of Hardware.
- Quick Bring up Test Program CTLab (GUI + CSV).
 ✓ Modify Timing Levels & Pattern to Debug DUT.
- Power vs Frequency Shmoo

✓ Capability to Shmoo Power vs Frequency.

• Faster Test Rates (100MHz vs 100KHz)

✓ Faster Pattern Execution.

• Floating Licenses - Everyone can use CTS.



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Next Steps

- Release Generic PMBus IPs
- GPIB Control For Power Supplies
- LabVIEW Control For Power Supplies

