SER Testing With Cloud Testing Service

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Outline

- Soft Error Rate Definition Of Terms
- SER Testing Requirements
- Cloud Testing Service Approach
- SER Testing Algorithm For Sram
- SER Testing Calculations
- Q&A And Wrap-up

Soft Errors

- **Soft error:** An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell --- **JESD89A**
- **Soft Error Rate Measured as FITs** (Failure in Time): The number of failures per 10^9 device hours.
- **1 year MTTF:** Equates to 114,155 FITs ($10^9/(24 \times 365)$)
- Four Pronged Approach to Soft Error Reduction
  1. Methods estimate the impact of soft errors (assessment).
  2. Methods to protect chips from soft errors (prevention).
  3. Methods to detect soft errors (testing).
  4. Methods to recover from soft errors (recovery).

NOTE: *Hard errors are irreversible changes in operation that are typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events). The error is "hard" because the data is lost and the component or device no longer functions properly, even after power reset and re-initialization.*

Soft Errors - Sources

- Spontaneous Changes in Digital Information Due to Radiation
  1. Alpha particles from uranium/thorium impurities in packaging materials
  2. High-energy (> 1 MeV) neutrons from cosmic radiation
     - Can induce soft errors in semiconductor devices via secondary ions produced by the neutron reaction with silicon nuclei.
  3. Secondary radiation from interaction of cosmic ray neutrons and boron (From the use of *Borophosphosilicate glass*).
     - BPSG commonly used as *p*-type dopant for junction formation in ICs
- By use of highly purified package materials and removal of BPSG SER due to 1 & 3 are greatly reduced
- Today High-energy cosmic rays are the major reasons for SER.
- *However an overall assessment of a device's soft error sensitivity is complete ONLY when the alpha AND high- and low-energy neutron induced failure rates have been accounted for.*

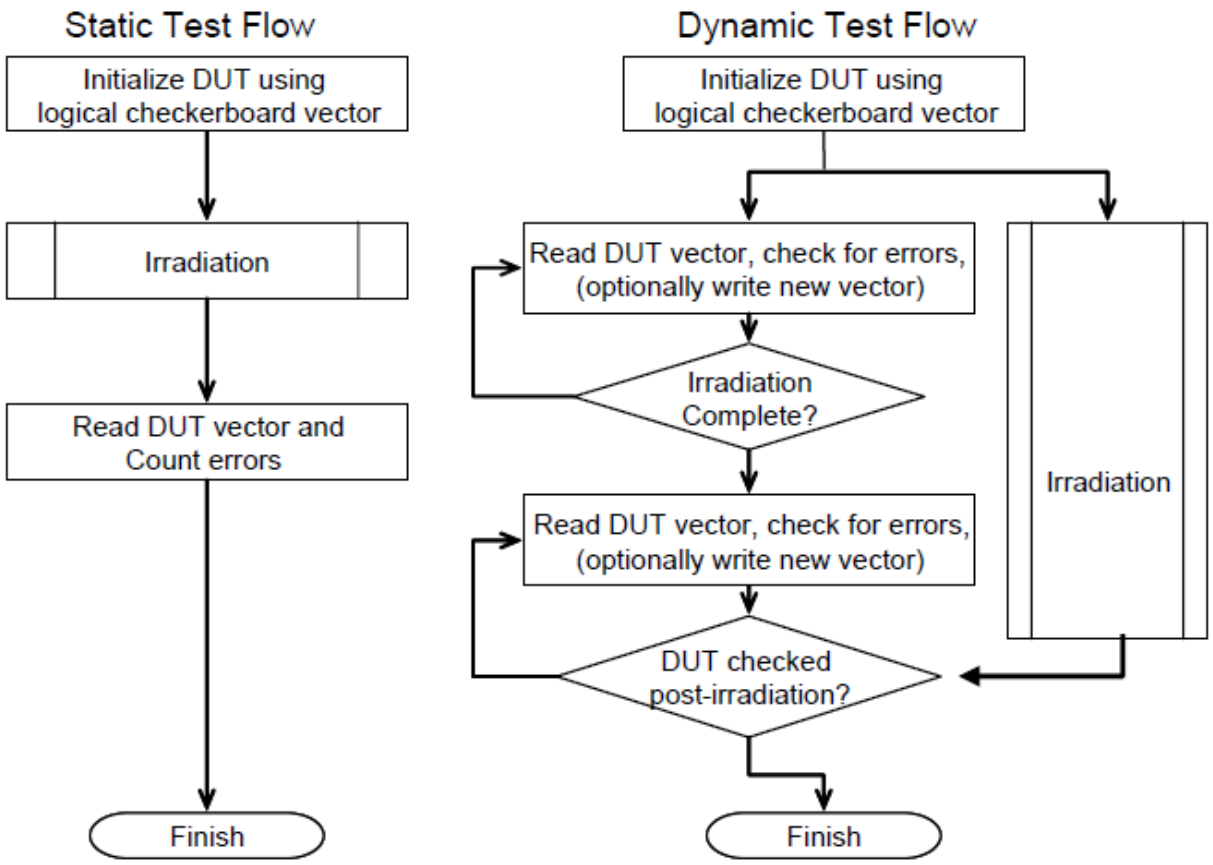
SER Testing Methods

- Real Time SER Test Procedure (Un-accelerated)
  - Measurement of Errors Under Normal Operation
    - Would Take a very long time with a single device
  - Today large number of devices are used in parallel
    - By using a server farm or a large system with a large device count
  - Testing also done at higher altitudes where higher rates occur
- Accelerated SER Tests With Automated Test Equipment
  - Using alpha particles to determine sensitivity to radioactive impurities
  - With high energy neutron beam to estimate sensitivity to background radiation
  - Under low energy neutron beam to estimate sensitivity to Boron10
- Pros/Cons of Each Method
  - RTSER has the advantage of being a direct measurement
  - RTSER is expensive- high number of units and the long time it takes
  - ASER needs just a few units and takes much shorter time
  - ASER has the disadvantage that the results need to be extrapolated

SER Testing Requirements

- ATE Needs to be Operated Remotely
  - To shield operator from radiation exposure
- Provide long cable to DUT fixture in the radiation chamber
- ATE should be compact and portable
  - The SER tests are conducted typically in a neutron/proton beam facility
  - The ATE and the associated device fixture need to be transported
  - The equipment should be operable from normal AC power
- In addition to the above, the following features are required:
  1. The ability to adjust and monitor the temperature of the DUT.
  2. Monitoring power supply current compliance to check for latch up.
  3. Operation at, or near, the rated DUT clock speed if test performed in dynamic mode.
  4. Provide error detection and logging without any omissions during system dead time.

SER Testing Static Vs Dynamic

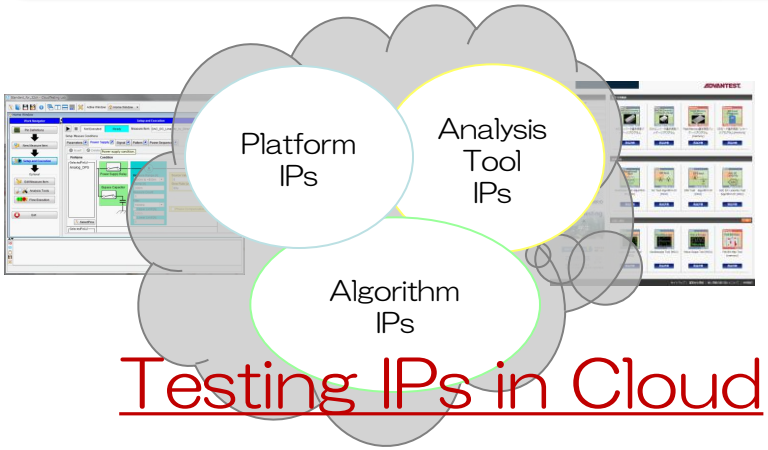


- Dynamic testing has to be planned to eliminate “dead-time” between a read of a location and a subsequent write to that location.
  - In order to prevent missing any error that occurs between a read from a location and the next write.
- Failure to account for this dead time will result in a lower estimate of SER.

Cloud Testing Service - Usage

Available whenever, wherever, whoever needs it, and easy to use!

CloudTesting™ Service

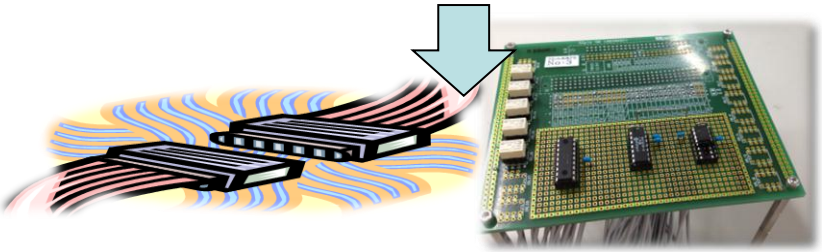


Testing IPs in Cloud

Purchase cables & the socket board on E-commerce site

Download IPs to your PC

USB



HW is rental contract

Small Foot Print

H/W : CloudTesting™ Station

1. Small footprint
   W107mm H198mm D400mm 6 Kg
   W4.2in H7.8in D15.7in 13 lb
2. Office power outlet
   100V-240V
3. Configurable architecture for various testing scenarios.
   - Measure passive/active semiconductor components
   - Design Verification of Logic Circuits.
   - Teaching Testing Classes at universities/colleges
   - For use in R&D of test circuits.

CX1000P

CX1000D

Resource Scaling

CX1000P

I/O:	32ch
DPS:	2ch
PMU:	1ch
AWG:	1ch
DGT:	1ch
RVS:	2ch

CX1000D

I/O:	128ch
DPS:	8ch
PMU:	4ch
AWG:	4ch
DGT:	4ch
RVS:	8ch

CX1000D S2-LINK

I/O:	256ch
DPS:	16ch
PMU:	8ch
AWG:	8ch
DGT:	8ch
RVS:	16ch

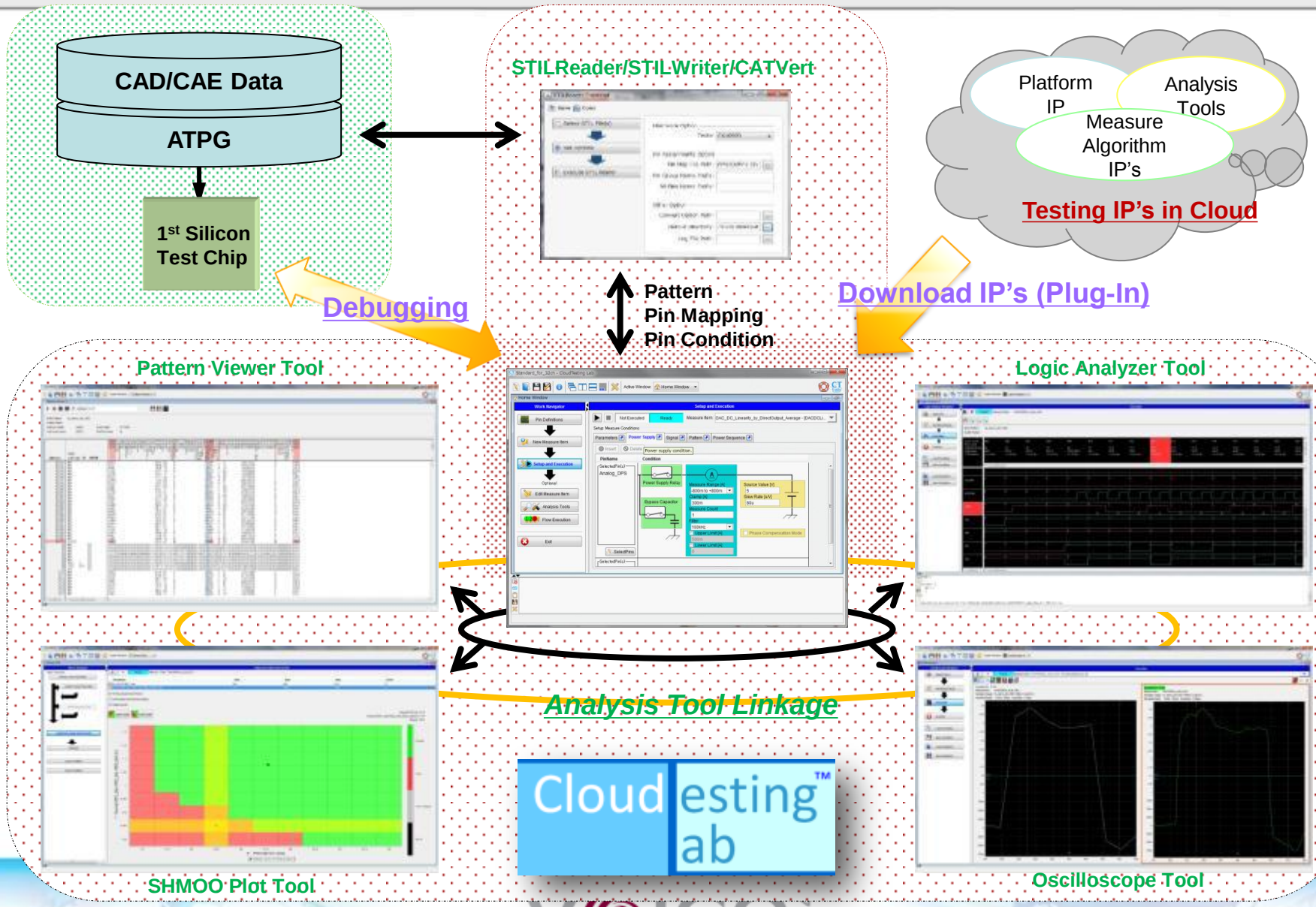
Long Tester Cables

Software Without Coding Efforts

S/W : CloudTesting™ Lab

1. GUI & CSV
   - Specify the test conditions by using GUI.
   - Set the test conditions by importing CSV.
   - No dedicated/specific programming language.
2. Plug-In architecture
   Testing/Tool IP work as plug-in.
3. EDA Linkage
   Support STIL (STILReader/Writer)
   and VCD/eVCD.
4. Windows7 64bit
   Mem: 4GB, HDD: > 30GB, USB2.0

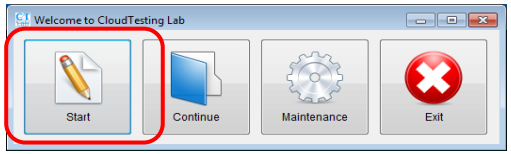
Cloud Testing Service – Tools Set



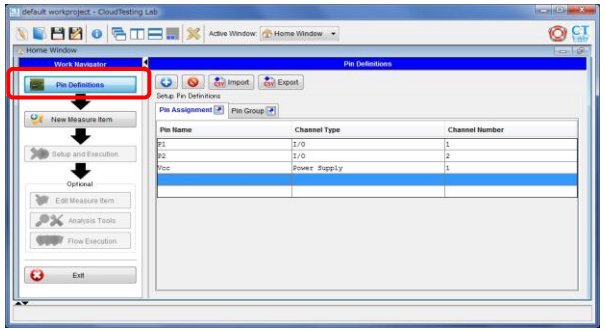
CTLAB Operations – Quick Program Setup

Execute DC Test/FT Test by only 4 steps!

1

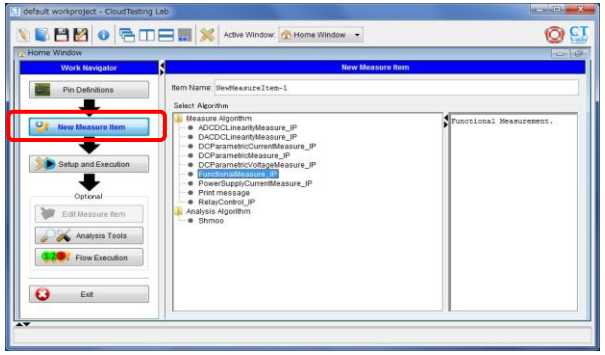


Start up Window



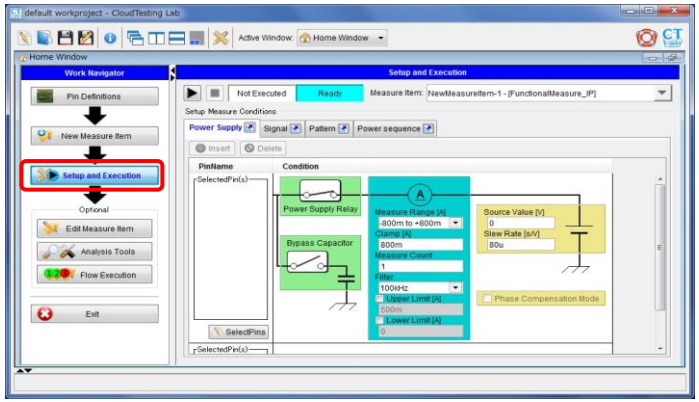
Specify Pin Definitions

2



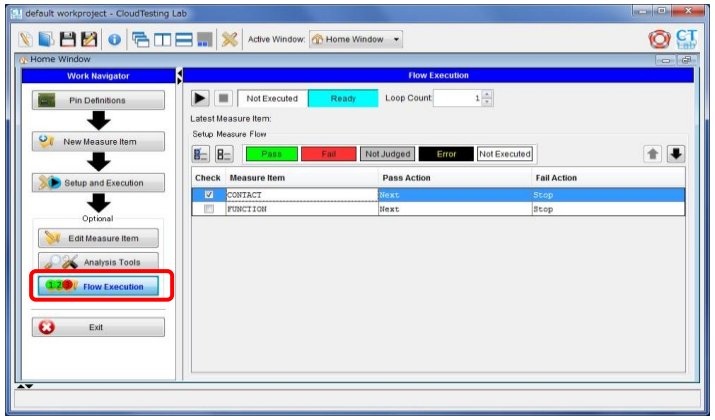
Select New Measure Item (IP)

3



Specify Setup and Execution

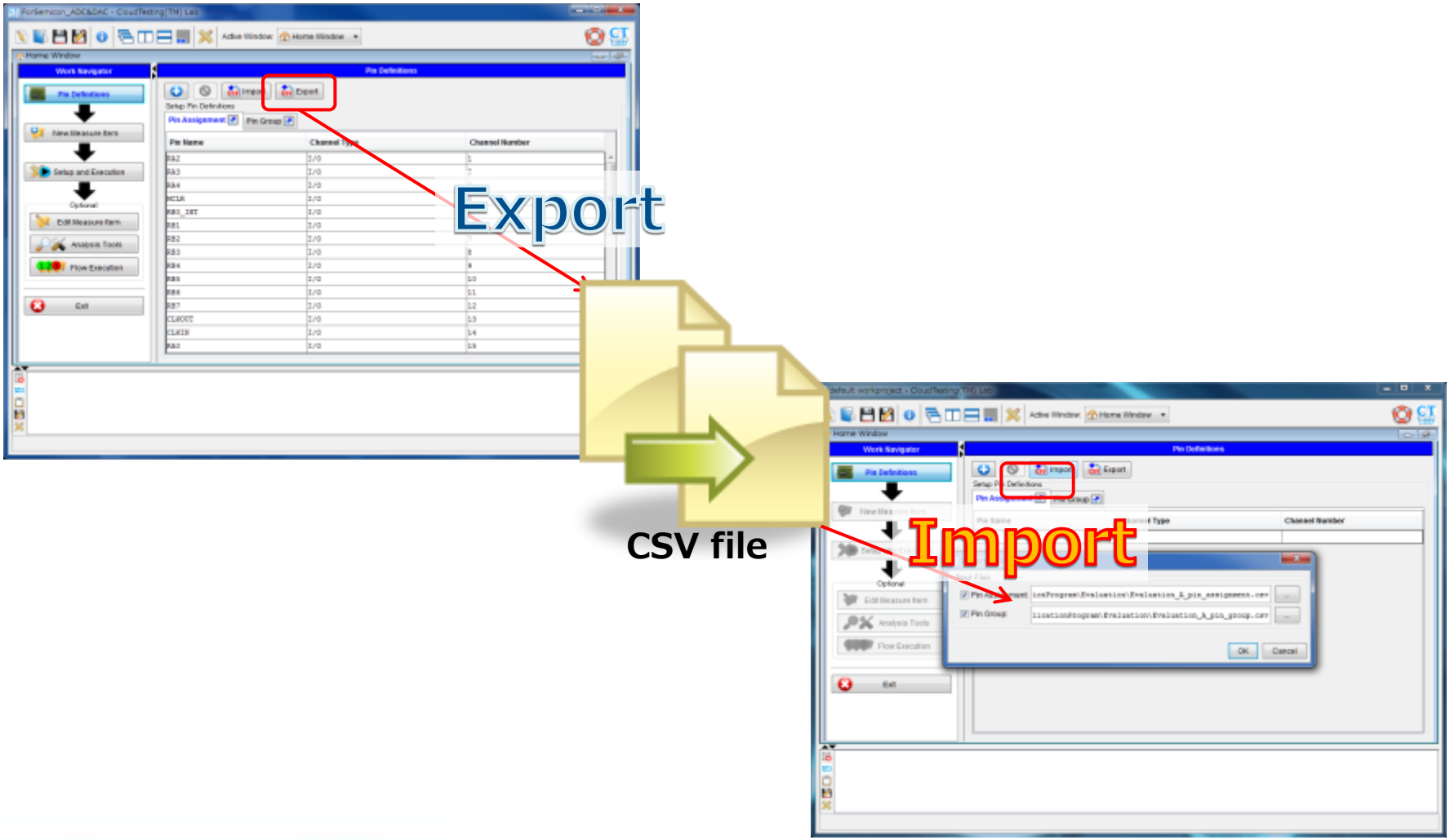
4



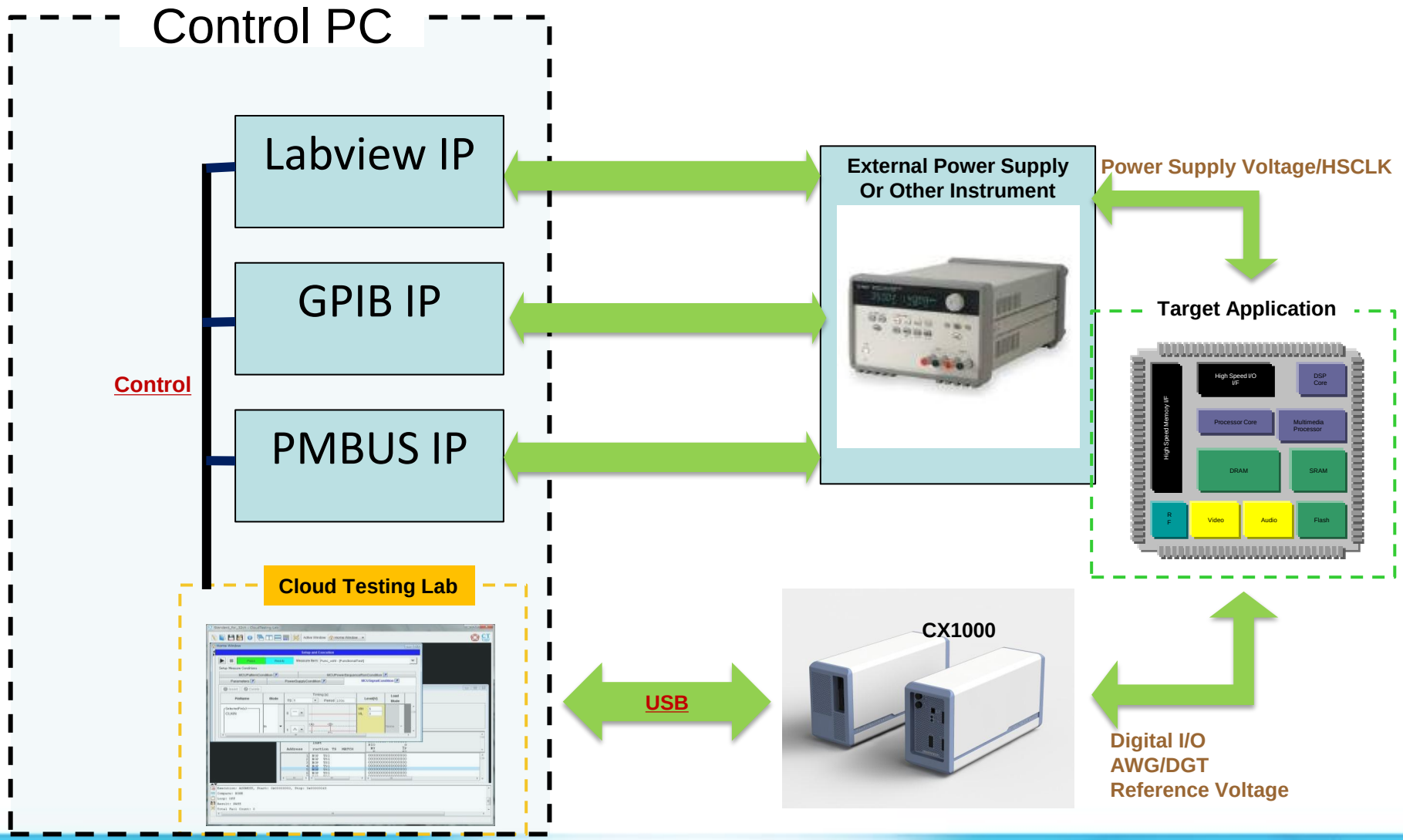
Specify Flow Execution

CTLAB Operations – Supports CSV

Import/Export pinmap definition and signal conditions by CSV format.



CTS – External Instrument Support



CTS Versus SER Testing Requirements

- ✓ Portable – Small Foot Print, Powered from wall outlet
- ✓ No Maintenance Charges –Replacement Unit Shipped Free
- ✓ Quick Bring up Test Program –CTLAB (GUI + CSV)
- ✓ Quick Bring up Patterns – STILReader (Provides Timing Too)
- ✓ Shielding From Radiation – Long Tester Cables (1m,3m,5m)

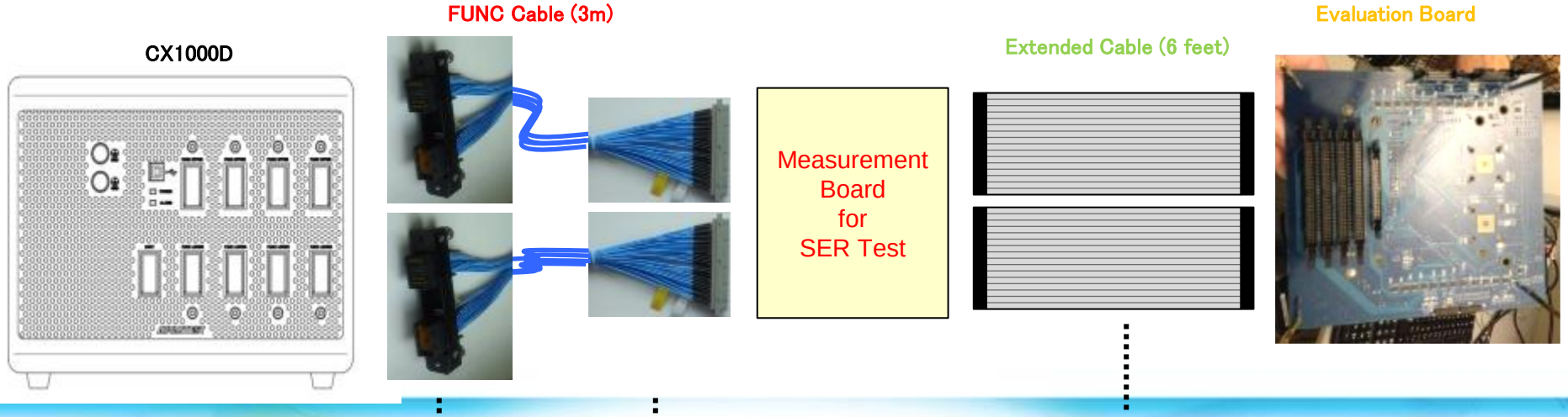
CTS SER Testing Setup For SRAM

- SER Testing Environment on CX1000D is required these items below :
  - CX1000D
  - Func Cable (3m), x 4 set
  - Cont Cable (3m), x 1 set
  - Measurement Board for SER Test
  - Extended Cable (6 feet)
  - Evaluation Board

Rental Contract

Purchase HW's

Existing HW's

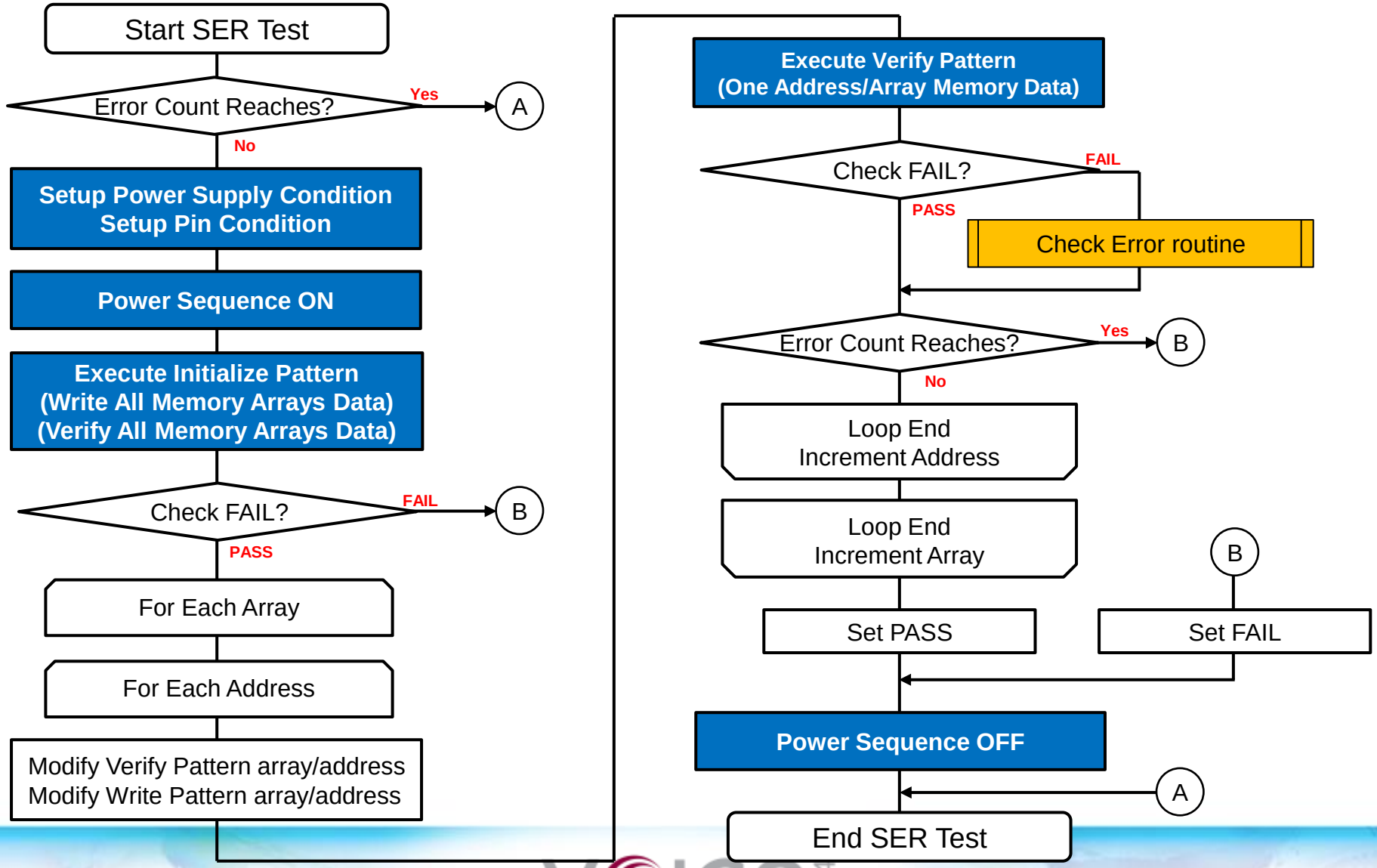


CTS SER Testing Setup For SRAM

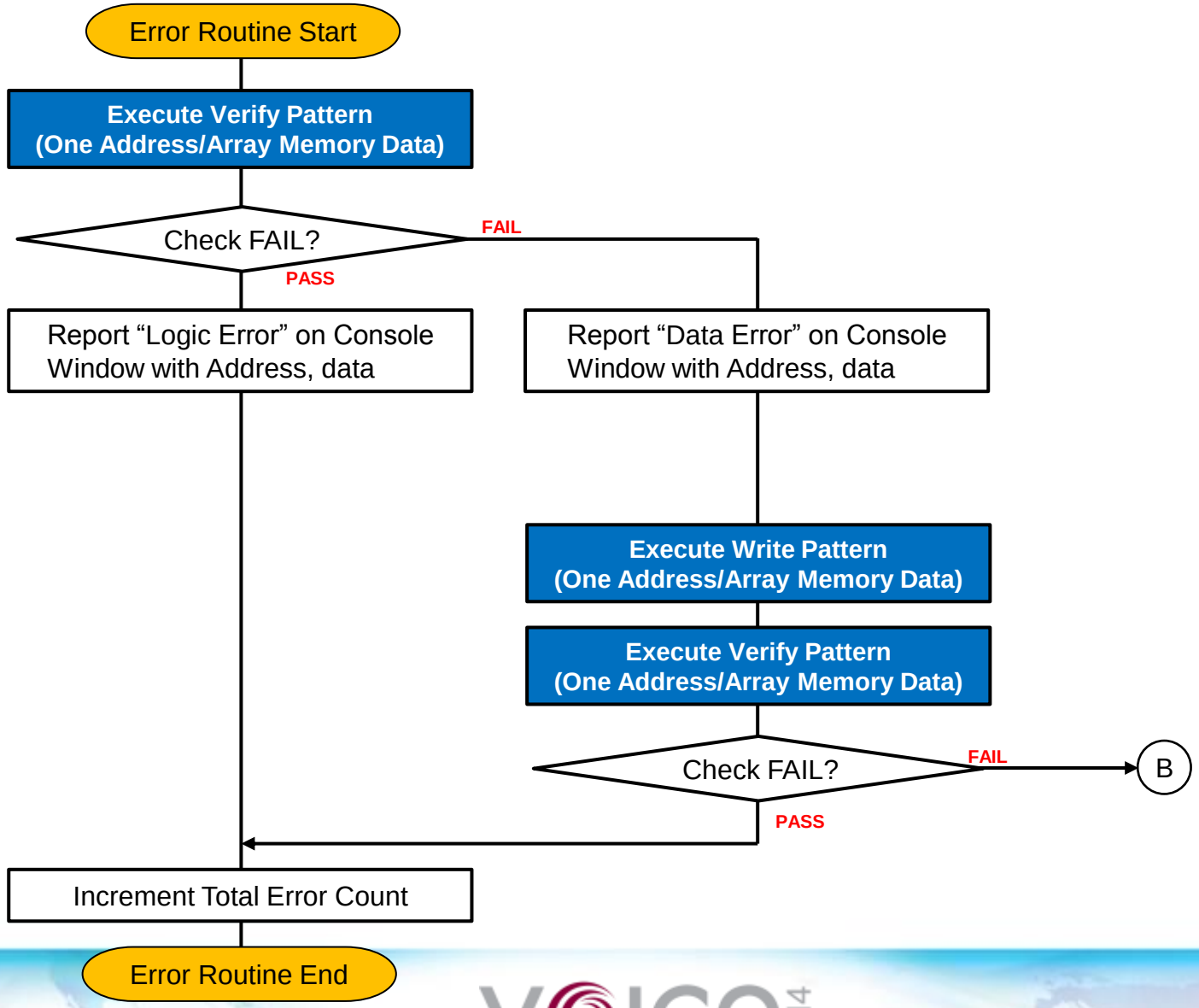
SRAM SER Memory Test Algorithm

1. Initialize the memory arrays by writing data patterns to arrays.
2. Verify data are ok.
3. Start the SER test loop:
   A) Until error count limit is reached, for each array, check the data for each address.
   B) If there is an error in the read-out for that address, then
      i. Read the data again to confirm the error is persistent
         a) If error is persistent, then report error as “Data Error” with logging of data address and data error pattern and write the correct data to the same address. Then read the data out to confirm that the correct data is written.
         b) If there is no error, then report error as “Logic Error” with logging of data address and data error pattern.
         c) Increment error count by number of error read in that address
      ii. Increment data address
      iii. Go to step A).

Memory SER Test on CX1000D, TEST FLOW



Memory SER Test on CX1000D, TEST FLOW



Memory SER Test on CX1000D, Specification

- SER Result Output format is contained the following information.
  - Header Information
    - [Test Description]
    - [Total Error Count] Maximum Error Count
  - Body Information
    - [Error Count] Current Error Count
    - [Verify Pattern Name]
    - [Message] “Data Error” or “Logic Error”
    - [Fail Array]
    - [Fail Address]
    - [Fail Data Pin Name]
    - [Fail Pattern Mnemonic]

```
[Test Desciption],[Total Error Count]
,,[Error Count],[Pattern Name],[Message],[Address],[Fail Data Pin],[Fail Mnemonic]
                    :::::::
```

Parameter Design (Condition Windows)

- Power Supply Condition Setting
  - Same as “FunctionalMeasurement_IP”
- Signal Condition Setting
  - Same as “FunctionalMeasurement_IP”
- Pattern Condition Setting (Initialize)
  - Define Write/Verify Memory Patterns (All of Memory Cells, Solid Data)
- Pattern Condition Setting (Verify)
  - Define Verify Memory Pattern (Just One Cell, Solid Data)
- Pattern Condition Setting (Write)
  - Define Write Memory Pattern (Just One Cell, Solid Data)
- Power Sequence Control Setting
  - Same as “FunctionalMeasurement_IP”

Parameter Design (Parameters Windows)

- Test Description
  - Define Test Description
- Array Pins
  - Define Array Pin Name (LSB First, exp. “a0,a1,a2”)
- Address Pins
  - Define Address Pin Name (LSB First, exp. “a3,a4,a5,a6,a7,a8,a9,…”)
- Maximum Error Count
  - Define Total Error Count
    - Positive Integer : Setting Maximum Error Count Value
    - “-1” : No Judgment
    - “0” : Continue previous SER Testing IP Value.
  - Default Setting is “0”.

Parameter Design (Parameters Windows)

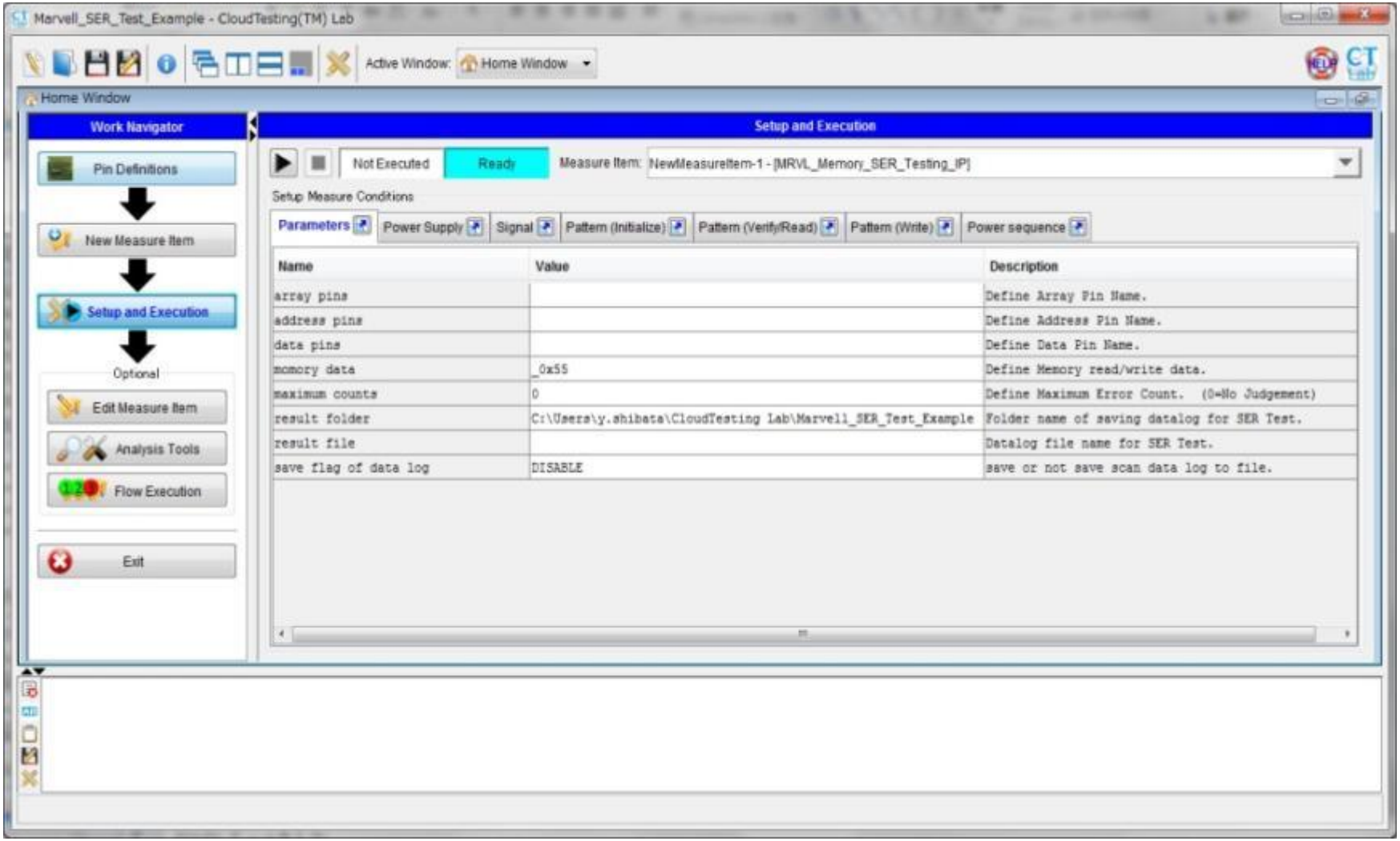
- Total Error Count Clear Mode
  - Define the mode whether Total Error Count Clear or No-Clear.
  - Default Setting is “No-Clear”.

- Result File Folder Name
  - Folder Name for Result Log Saving.
  - Default Setting is “C:¥Users¥[User Name]¥CloudTesting Lab¥[Work Project]”

- Result File Name
  - Result Log File Name.

- Enable/Disable for Saving Result File
  - Enable/Disable Flag of Result Log Saving.
  - Default Setting is “DISABLE”.

CX1000 SER Test Condition Image



SER Calculation From Tester Datalog

Alpha Particle Source: ASER is Tester Observed Fails In FITs

$$\text{Un-accelerated SER} = \frac{(F_{pkg}).(F_{geopkg}).(F_{shieldpkg})}{(F_{dut}).(F_{geodut}).(F_{shielddut})} \cdot \text{ASER}$$

Spallation Neutron Beam Source: N_{seu} is Tester Observed Fails in FITs

$$\text{Un-accelerated SER} = 3.6 \times 10^{-3} \times \overline{\sigma_{SEU\text{-}bit}}$$

$$\sigma_{SEU\text{-}bit} = N_{seu} / (F_{spec} \times N_{bit})$$